

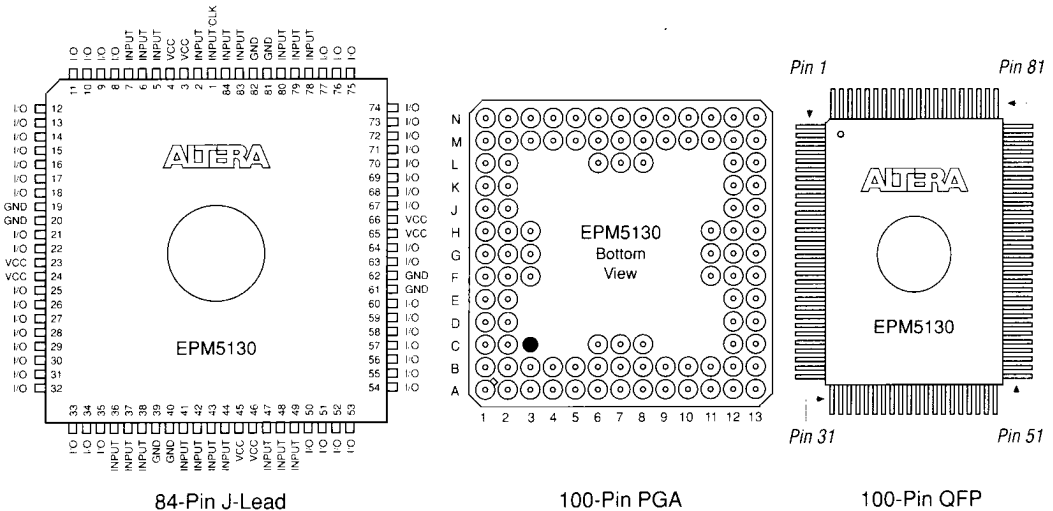
# EPM5130 EPLD

## Features

- ❑ High-density, 128-macrocell, general-purpose MAX 5000 EPLD
- ❑ 128 macrocells optimized for pin-intensive applications, easily integrating over 60 TTL MSI and SSI components
- ❑ High-speed multi-LAB architecture
  - $t_{PD}$  as fast as 25 ns
  - Counter frequencies up to 50 MHz
  - Pipelined data rates up to 62.5 MHz
- ❑ High pin count for 16- or 32-bit data paths
- ❑ 256 shareable expander product terms (“expanders”) allowing over 32 product terms in a single macrocell
- ❑ 20 high-speed dedicated inputs for fast latching of 16-bit functions
- ❑ Fast Clock-to-output delays for bus-oriented functions
- ❑ Programmable I/O architecture allowing up to 84 inputs or 64 outputs in 100-pin packages, or up to 68 inputs or 48 outputs in 84-pin packages
- ❑ Available in windowed ceramic and one-time-programmable (OTP) packages (see Figure 22):
  - 84-pin J-lead chip carrier (JLCC and PLCC)
  - 100-pin pin-grid array (ceramic PGA only)
  - 100-pin quad flat pack (CQFP and PQFP)

**Figure 22. EPM5130 Package Pin-Out Diagrams**

Package outlines not drawn to scale. See Tables 5 and 6 in this data sheet for pin-out information. Windows in ceramic packages only.



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## General Description

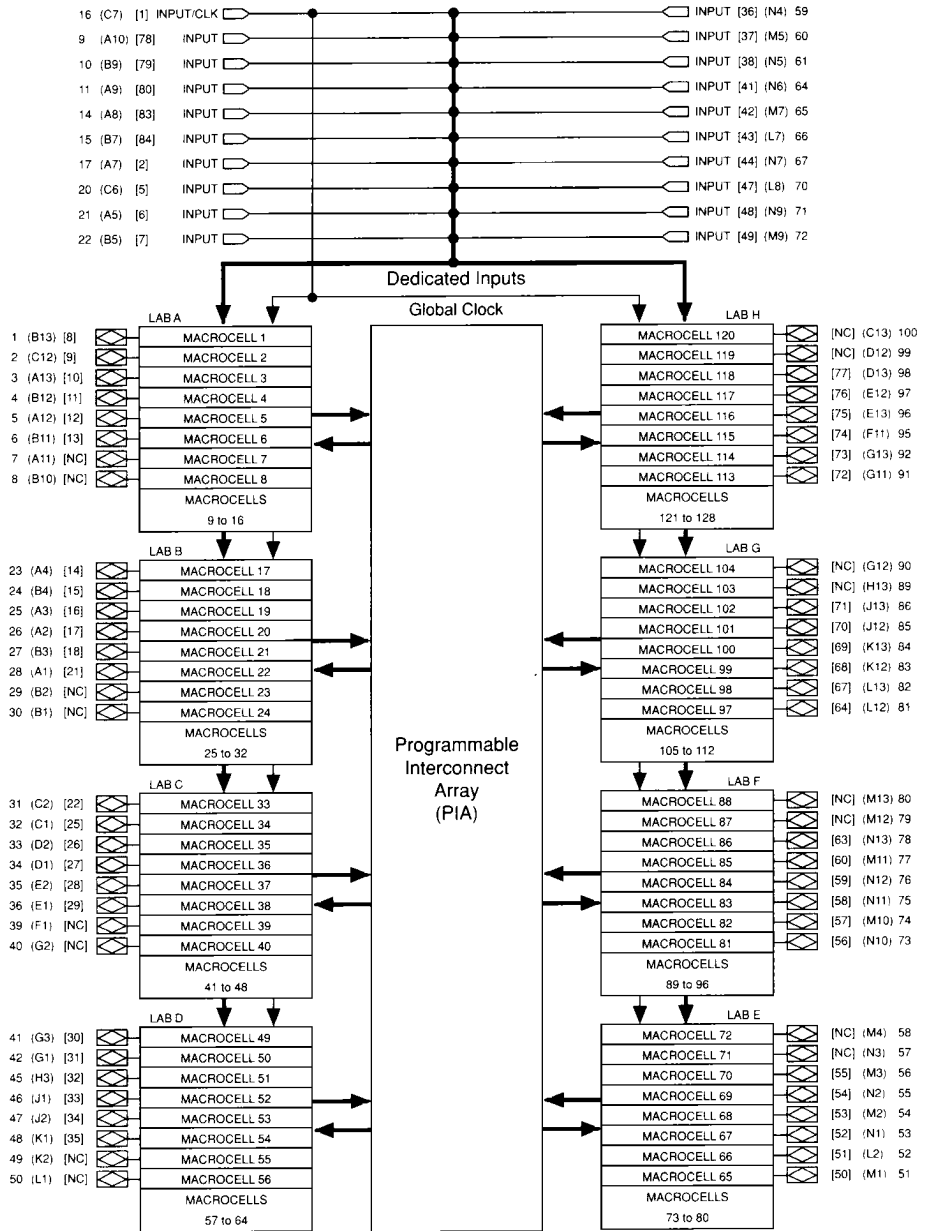
The Altera EPM5130 EPLD is a user-configurable, high-performance MAX 5000 EPLD optimized for pin-intensive designs. It provides a high-density replacement for 74-series SSI and MSI TTL and CMOS logic. A single EPM5130 EPLD can quickly integrate multiple 20- and 24-pin low-density PLDs and high-pin-count subsystems, such as custom DMA controllers. In addition, it can handle a 32-bit data path application with enough I/O to allow the required control signals to be implemented.

The EPM5130 consists of 128 macrocells equally divided into 8 Logic Array Blocks (LABs), each containing 16 macrocells and 32 expander product terms. Expander product terms can be used and shared by all macrocells in the device to ensure efficient use of device resources. Because the LAB is very compact, the high speeds required by most I/O subsystems are maintained. See Figure 23.

The EPM5130 has 20 dedicated input pins that allow high-speed input latching of 16-bit functions. One of these inputs can be configured as a global Clock to provide enhanced Clock-to-output delays for bus-oriented functions. The EPM5130 also has 64 I/O pins, 8 in each LAB, that can be configured for input, output, or bidirectional operation. Dual feedback on the I/O pins provides the most efficient use of device pin resources.

Figure 23. EPM5130 Block Diagram

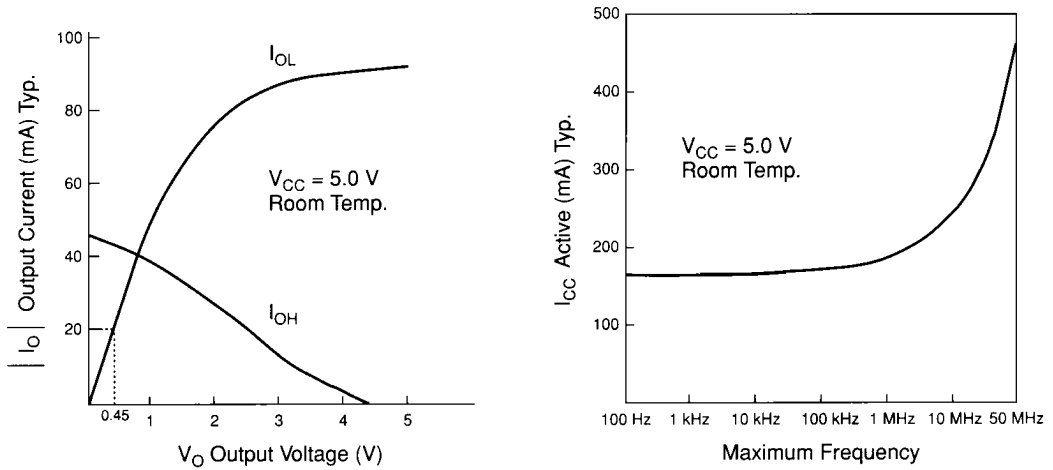
Numbers without parentheses are for J-lead packages; numbers in parentheses are for PGA packages; numbers in brackets are for QFP packages.



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Figure 24 shows the output drive characteristics of EPM5130 I/O pins and typical supply current ( $I_{CC}$ ) versus frequency for the EPM5130.

**Figure 24. EPM5130 Maximum Output Drive Characteristics &  $I_{CC}$  vs. Frequency**



**Absolute Maximum Ratings** See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	Supply voltage	With respect to GND	-2.0	7.0	V
$V_{PP}$	Programming supply voltage	Note (1)	-2.0	13.5	V
$V_I$	DC input voltage		-2.0	7.0	V
$I_{MAX}$	DC $V_{CC}$ or GND current				500
$I_{OUT}$	DC output current, per pin		-25	25	mA
$P_D$	Power dissipation			2500	mW
$T_{STG}$	Storage temperature	No bias	-65	150	°C
$T_{AMB}$	Ambient temperature	Under bias, Note (2)	-65 [-55]	135 [125]	°C
$T_J$	Junction temperature	Under bias, Note (2)		150 [175]	°C

### Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	Supply voltage	Note (3)	4.75 (4.5)	5.25 (5.5)	V
$V_I$	Input voltage		0	$V_{CC}$	V
$V_O$	Output voltage		0	$V_{CC}$	V
$T_A$	Operating temperature	For commercial use	0	70	°C
$T_A$	Operating temperature	For industrial use	-40	85	°C
$T_C$	Case temperature	For military use	-55	125	°C
$t_R$	Input rise time			100	ns
$t_F$	Input fall time			100	ns

**DC Operating Conditions** Notes (4), (5)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IH}$	High-level input voltage	Note (2)	2.0 [2.2]		$V_{CC} + 0.3$	V
$V_{IL}$	Low-level input voltage		-0.3		0.8	V
$V_{OH}$	High-level TTL output voltage	$I_{OH} = -4$ mA DC	2.4			V
$V_{OL}$	Low-level output voltage	$I_{OL} = 8$ mA DC			0.45	V
$I_I$	Input leakage current	$V_I = V_{CC}$ or GND	-10		10	μA
$I_{OZ}$	Tri-state output off-state current	$V_O = V_{CC}$ or GND	-40		40	μA
$I_{CC1}$	$V_{CC}$ supply current (standby)	$V_I = V_{CC}$ or GND, Notes (3), (6)		175	250 (325)	mA
$I_{CC3}$	$V_{CC}$ supply current (active)	$V_I = V_{CC}$ or GND, No load, $f = 1.0$ MHz, Notes (3), (6)		180	275 (375)	mA

### Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
$C_{IN}$	Input capacitance	$V_{IN} = 0$ V, $f = 1.0$ MHz		10	pF
$C_{OUT}$	Output capacitance	$V_{OUT} = 0$ V, $f = 1.0$ MHz		20	pF

**AC Operating Conditions** Note (5)

<b>External Timing Parameters</b>			EPM5130-1		EPM5130-2		EPM5130		
<b>Symbol</b>	<b>Parameter</b>	<b>Conditions</b>	<b>Min</b>	<b>Max</b>	<b>Min</b>	<b>Max</b>	<b>Min</b>	<b>Max</b>	<b>Unit</b>
$t_{PD1}$	Input to non-registered output	C1 = 35 pF		25		30		35	ns
$t_{PD2}$	I/O input to non-registered output			40		45		55	ns
$t_{SU}$	Global clock setup time		15		20		25	ns	
$t_H$	Global clock hold time		0		0		0	ns	
$t_{CO1}$	Global clock to output delay	C1 = 35 pF		14		16		20	ns
$t_{CH}$	Global clock high time		8		10		12.5	ns	
$t_{CL}$	Global clock low time		8		10		12.5	ns	
$t_{ASU}$	Array clock setup time		5		6		10	ns	
$t_{AH}$	Array clock hold time		6		8		10	ns	
$t_{ACO1}$	Array clock to output delay	C1 = 35 pF		25		30		35	ns
$t_{ACH}$	Array clock high time	Note (7)	11		14		16		ns
$t_{ACL}$	Array clock low time		9		11		14		ns
$t_{CNT}$	Minimum global clock period			20		25		30	ns
$f_{CNT}$	Max. internal global clock frequency	Note (6)	50		40		33.3		MHz
$t_{ACNT}$	Minimum array clock period			20		25		30	ns
$f_{ACNT}$	Max. internal array clock frequency	Note (6)	50		40		33.3		MHz
$f_{MAX}$	Maximum clock frequency	Note (8)	62.5		50		40		MHz

<b>Internal Timing Parameters</b> Note (9)			EPM5130-1		EPM5130-2		EPM5130		
<b>Symbol</b>	<b>Parameter</b>	<b>Conditions</b>	<b>Min</b>	<b>Max</b>	<b>Min</b>	<b>Max</b>	<b>Min</b>	<b>Max</b>	<b>Unit</b>
$t_{IN}$	Input pad and buffer delay			5		7		11	ns
$t_{IO}$	I/O input pad and buffer delay			6		6		11	ns
$t_{EXP}$	Expander array delay			12		14		20	ns
$t_{LAD}$	Logic array delay			12		14		14	ns
$t_{LAC}$	Logic control array delay			10		12		13	ns
$t_{OD}$	Output buffer and pad delay	C1 = 35 pF		5		5		6	ns
$t_{ZX}$	Output buffer enable delay				10		11		13
$t_{XZ}$	Output buffer disable delay	C1 = 5 pF		10		11		13	ns
$t_{SU}$	Register setup time		6		8		12		ns
$t_{LATCH}$	Flow-through latch delay			3		4		4	ns
$t_{RD}$	Register delay			1		2		2	ns
$t_{COMB}$	Combinatorial delay			3		4		4	ns
$t_H$	Register hold time		4		6		8		ns
$t_{IC}$	Array clock delay			14		16		16	ns
$t_{ICS}$	Global clock delay			3		2		1	ns
$t_{FD}$	Feedback delay			1		1		2	ns
$t_{PRE}$	Register preset time			5		6		7	ns
$t_{CLR}$	Register clear time			5		6		7	ns
$t_{PIA}$	Prog. Interconnect Array delay			14		16		20	ns

**Notes to tables:**

- (1) Minimum DC input is  $-0.3\text{ V}$ . During transitions, the inputs may undershoot to  $-2.0\text{ V}$  or overshoot to  $7.0\text{ V}$  for periods shorter than  $20\text{ ns}$  under no-load conditions.
- (2) Numbers in brackets are for MIL-STD-883-compliant versions only.
- (3) Numbers in parentheses are for military- and industrial-temperature-range versions, as well as for MIL-STD-883-compliant versions.
- (4) Typical values are for  $T_A = 25^\circ\text{ C}$  and  $V_{CC} = 5\text{ V}$ .
- (5) Operating conditions:  $V_{CC} = 5\text{ V} \pm 5\%$ ,  $T_A = 0^\circ\text{ C}$  to  $70^\circ\text{ C}$  for commercial use.  
 $V_{CC} = 5\text{ V} \pm 10\%$ ,  $T_A = -40^\circ\text{ C}$  to  $85^\circ\text{ C}$  for industrial use.  
 $V_{CC} = 5\text{ V} \pm 10\%$ ,  $T_C = -55^\circ\text{ C}$  to  $125^\circ\text{ C}$  for military use.
- (6) Measured with a 16-bit counter programmed into each LAB.  $I_{CC}$  measured at  $0^\circ\text{ C}$ .
- (7) This parameter is measured with a positive-edge-triggered Clock at the register. For negative-edge clocking, the  $t_{ACH}$  and  $t_{ACL}$  parameters must be swapped.
- (8) The  $f_{MAX}$  values represent the highest frequency for pipelined data.
- (9) For information on internal timing parameters, refer to *Application Brief 100 (Understanding EPLD Timing)* in this data book.

## Product Availability

Product Grade		Availability
Commercial Temp.	( $0^\circ\text{ C}$ to $70^\circ\text{ C}$ )	EPM5130-1, EPM5130-2, EPM5130
Industrial Temp.	( $-40^\circ\text{ C}$ to $85^\circ\text{ C}$ )	EPM5130
Military Temp.	( $-55^\circ\text{ C}$ to $125^\circ\text{ C}$ )	EPM5130
MIL-STD-883-Compliant	Note (1)	See <i>Military Products</i> in this data book.

**Note:**

- (1) MIL-STD-883-compliant product specifications are provided in this data book and in Military Product Drawings (MPDs). However, only MPDs should be used to prepare Source Control Drawings (SCDs). MPDs are available from Altera Marketing at (408) 894-7000.

## Pin-Out Information

Tables 5 and 6 provide pin-out information for the EPM5130.

Dedicated Pin	84-Pin J-Lead	100-Pin PGA	100-Pin QFP
INPUT/CLK	1	C7	16
INPUT	2, 5, 6, 7, 36, 37, 38, 41, 42, 43, 44, 47, 48, 49, 78, 79, 80, 83, 84	A5, A7, A8, A9, A10, B5, B7, B9, C6, L7, L8, M5, M7, M9, N4, N5, N6, N7, N9	9, 10, 11, 14, 15, 16, 17, 20, 21, 22, 59, 60, 61, 64, 65, 66, 67, 70, 71, 72
GND	19, 20, 39, 40, 61, 62, 81, 82	B8, C8, F2, F3, H11, H12, L6, M6	12, 13, 37, 38, 62, 63, 87, 88
VCC	3, 4, 23, 24, 45, 46, 65, 66	A6, B6, F12, F13, H1, H2, M8, N8	18, 19, 43, 44, 68, 69, 93, 94

Table 6. EPM5130 I/O Pin-Outs (Part 1 of 2)

MC	LAB	84-Pin J-Lead	100-Pin PGA	100-Pin QFP	MC	LAB	84-Pin J-Lead	100-Pin PGA	100-Pin QFP
1	A	8	B13	1	17	B	14	A4	23
2	A	9	C12	2	18	B	15	B4	24
3	A	10	A13	3	19	B	16	A3	25
4	A	11	B12	4	20	B	17	A2	26
5	A	12	A12	5	21	B	18	B3	27
6	A	13	B11	6	22	B	21	A1	28
7	A	–	A11	7	23	B	–	B2	29
8	A	–	B10	8	24	B	–	B1	30
9	A	–	–	–	25	B	–	–	–
10	A	–	–	–	26	B	–	–	–
11	A	–	–	–	27	B	–	–	–
12	A	–	–	–	28	B	–	–	–
13	A	–	–	–	29	B	–	–	–
14	A	–	–	–	30	B	–	–	–
15	A	–	–	–	31	B	–	–	–
16	A	–	–	–	32	B	–	–	–
33	C	22	C2	31	49	D	30	G3	41
34	C	25	C1	32	50	D	31	G1	42
35	C	26	D2	33	51	D	32	H3	45
36	C	27	D1	34	52	D	33	J1	46
37	C	28	E2	35	53	D	34	J2	47
38	C	29	E1	36	54	D	35	K1	48
39	C	–	F1	39	55	D	–	K2	49
40	C	–	G2	40	56	D	–	L1	50
41	C	–	–	–	57	D	–	–	–
42	C	–	–	–	58	D	–	–	–
43	C	–	–	–	59	D	–	–	–
44	C	–	–	–	60	D	–	–	–
45	C	–	–	–	61	D	–	–	–
46	C	–	–	–	62	D	–	–	–
47	C	–	–	–	63	D	–	–	–
48	C	–	–	–	64	D	–	–	–



Table 6. EPM5130 I/O Pin-Outs (Part 2 of 2)

MC	LAB	84-Pin J-Lead	100-Pin PGA	100-Pin QFP	MC	LAB	84-Pin J-Lead	100-Pin PGA	100-Pin QFP
65	E	50	M1	51	81	F	56	N10	73
66	E	51	L2	52	82	F	57	M10	74
67	E	52	N1	53	83	F	58	N11	75
68	E	53	M2	54	84	F	59	N12	76
69	E	54	N2	55	85	F	60	M11	77
70	E	55	M3	56	86	F	63	N13	78
71	E	-	N3	57	87	F	-	M12	79
72	E	-	M4	58	88	F	-	M13	80
73	E	-	-	-	89	F	-	-	-
74	E	-	-	-	90	F	-	-	-
75	E	-	-	-	91	F	-	-	-
76	E	-	-	-	92	F	-	-	-
77	E	-	-	-	93	F	-	-	-
78	E	-	-	-	94	F	-	-	-
79	E	-	-	-	95	F	-	-	-
80	E	-	-	-	96	F	-	-	-
97	G	64	L12	81	113	H	72	G11	91
98	G	67	L13	82	114	H	73	G13	92
99	G	68	K12	83	115	H	74	F11	95
100	G	69	K13	84	116	H	75	E13	96
101	G	70	J12	85	117	H	76	E12	97
102	G	71	J13	86	118	H	77	D13	98
103	G	-	H13	89	119	H	-	D12	99
104	G	-	G12	90	120	H	-	C13	100
105	G	-	-	-	121	H	-	-	-
106	G	-	-	-	122	H	-	-	-
107	G	-	-	-	123	H	-	-	-
108	G	-	-	-	124	H	-	-	-
109	G	-	-	-	125	H	-	-	-
110	G	-	-	-	126	H	-	-	-
111	G	-	-	-	127	H	-	-	-
112	G	-	-	-	128	H	-	-	-

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